EGCP281 Assignment #2

Submit only one zip file containing:

a) Your report in pdf format, and
b) A plain text README.TXT file which contains any comments or introductory information regarding your project

Submit in Titanium before deadline at midnight feb-24-2016. Late submission will automatically result in zero credit.

This assignment requires that you design a total of two circuits described below.

1. **Circuit 1:** Design a circuit that provides the 2's complement at its output for each 3-bit signed binary number applied at its input.
    - Use the input signals X, Y, and Z and the corresponding output signals F1, F2, and F3.
    - Use an output signal V which is set to 1 if the output signed number results in an over overflow, and 0 otherwise.
    - Use only AND, OR, and NOT gates.
    - Your report must show:
        i. The truth table of the circuit
        ii. The Boolean equations for each of the output signals as function of the input signal(s)
        iii. The circuit schematic diagram
        iv. The complete VHDL code
        v. The complete VHDL simulation screen captures
        vi. Your comments (what have you learned from this exercise? what were the challenges, and how did you overcome those challenges?

2. **Circuit 2:** Design a circuit that provides the majority of 1s circuit such that its output signal F is 1 when a majority of the input signals X, Y, and Z are 1.
    - Use only AND, OR, and NOT gates.
    - Your report must show:
        i. The truth table of the circuit
        ii. The Boolean equations for the output signal F as a function of the input signals
        iii. The circuit schematic diagram
        iv. The complete VHDL code
        v. The complete VHDL simulation screen captures
        vi. Your comments (what have you learned from this exercise? what were the challenges, and how did you overcome those challenges?